Microprocessor

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Lecture 3
Review

What are the four operations commonly performed by the MPU?

- Memory Read
  - Reads instructions or data from the memory
- Memory Write
  - Writes instructions and data into memory
- I/O Read
  - Accepts data from input devices
- I/O Write
  - Writes data to output devices
What is the function of address Bus?
- Holds memory or I/O addresses

How many memory locations can addressed by the MPU with 13 address lines?
- $2^{13}$

How many address lines are necessary to address two MB with 8-bit word size?
- 21 lines
Question

- Specify the number of Registers and Memory cells in a 128 X 4 memory chip?
  - 128 registers and 4 memory cells per register

- How many bits are stored by a 256 X 4 memory chip? Can this chip specified as 128-byte memory?
  - 256*4
  - No
Question

- If the memory chip size is 1024 X 4 bits, how many chips are required to make 4K (4096) bytes of memory?

- Two chips forms 1K memory
- We need 8 chips
Question

- Given the following Figure, define
- How many words?
- How many bit per word?
- How many address lines are used?
- What is the name of the used bus?

Diagram:
- CPU
  - 16 bit BUS
- Memory
  - 1024 X 16
State the steps required by the MPU to read or write from the memory?
How the MPU Writes into the Memory?

- MPU places the 16 bit address on the address bus
  - Memory interfacing circuits will decode address to specify the target register

- MPU Places a byte on the data bus

- MPU sends a control signal (Memory Write) to the memory to write
How the MPU reads from the Memory?

- MPU places the 16 bit address on the address bus
  - Memory interfacing circuits will decode address to specify the target register

- MPU sends a control signal (Memory Read) to the memory to enable the output buffer

- The memory puts the data on the data bus and the processor will read it
Define the following terms:

- Byte addressing
- Hit
- Miss
- SSI
- VLSI
- EBCDIC
- ASCII
- Compiler
Z80 Microprocessor Architecture
Z80 Hardware and programming Model

- 8-bit Microprocessor
- 16-bit address lines
- +5 V Power Supply
- Housed in 40 pin dual in Line (DIP) – 2 sides
- different versions of Z80 microprocessors such as Z80, Z80A, Z80B and Z80H
- rated to operate at various frequencies ranging from 2.5MHz to 8MHz.
# Z80 Pin Configuration

<table>
<thead>
<tr>
<th>Pin</th>
<th>Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_{11}</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>A_{12}</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>A_{13}</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>A_{14}</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>A_{15}</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Φ</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>D_{4}</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>D_{3}</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>D_{2}</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>D_{1}</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>+5 V</td>
<td>11</td>
<td></td>
</tr>
<tr>
<td>D_{7}</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>D_{7}</td>
<td>13</td>
<td></td>
</tr>
<tr>
<td>D_{0}</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>D_{1}</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>INT</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>NMI</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>HALT</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>MREQ</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>IORQ</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>22</td>
<td>WR</td>
</tr>
<tr>
<td>23</td>
<td>23</td>
<td>BUSAK</td>
</tr>
<tr>
<td>24</td>
<td>24</td>
<td>WAIT</td>
</tr>
<tr>
<td>25</td>
<td>25</td>
<td>BUSRQ</td>
</tr>
<tr>
<td>26</td>
<td>26</td>
<td>RESET</td>
</tr>
<tr>
<td>27</td>
<td>27</td>
<td>M_1</td>
</tr>
<tr>
<td>28</td>
<td>28</td>
<td>RFSH</td>
</tr>
<tr>
<td>29</td>
<td>29</td>
<td>GND</td>
</tr>
<tr>
<td>30</td>
<td>30</td>
<td>A_0</td>
</tr>
<tr>
<td>31</td>
<td>31</td>
<td>A_1</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>A_2</td>
</tr>
<tr>
<td>33</td>
<td>33</td>
<td>A_3</td>
</tr>
<tr>
<td>34</td>
<td>34</td>
<td>A_4</td>
</tr>
<tr>
<td>35</td>
<td>35</td>
<td>A_5</td>
</tr>
<tr>
<td>36</td>
<td>36</td>
<td>A_6</td>
</tr>
<tr>
<td>37</td>
<td>37</td>
<td>A_7</td>
</tr>
<tr>
<td>38</td>
<td>38</td>
<td>A_8</td>
</tr>
<tr>
<td>39</td>
<td>39</td>
<td>A_9</td>
</tr>
<tr>
<td>40</td>
<td>40</td>
<td>A_{10}</td>
</tr>
</tbody>
</table>

**FIGURE**

Z80 Microprocessor Pinout and Logic Signals

SOURCE: Courtesy of Zilog Corporation
Z80 Pin Configuration

System Control
- M1
- MREQ
- IORQ
- RD
- WR
- RFSH

CPU Control
- HALT
- WAIT
- INT
- NMI

CPU Bus Control
- RESET
- BUSRQ
- BUSACK

Address Bus
- 30
- 31
- 32
- 33
- 34
- 35
- 36
- 37
- 38
- 39
- 40
- 1
- 2
- 3
- 4
- 5
- A0
- A1
- A2
- A3
- A4
- A5
- A6
- A7
- A8
- A9
- A10
- A11
- A12
- A13
- A14
- A15

Data Bus
- 14
- 15
- 12
- 8
- 7
- 9
- 10
- 13
- D0
- D1
- D2
- D3
- D4
- D5
- D6
- D7
Signal Classification

- All the signals can be classified into six groups.
  - address bus
  - data bus
  - control signals
  - external requests
  - request acknowledge and special signals
  - power and frequency signals
Address Bus

- 16 tri-state signal lines, A15 – A0
- unidirectional and capable of addressing 64K \(2^{16}\) memory registers
- used to send (or place) the addresses of memory registers and I/O devices.

- Tri state (0, 1, high impedance (the output has no effect)
Data Bus

- eight tri-state bidirectional lines D7 – D0
- used for data transfer.
- data can flow in either direction—from the microprocessor to memory and I/Os or vice versa.
Control and Status Signals

- Five individual output lines:
  - three can be classified as status signals indicating the nature of the operation being performed,
  - two as control signals to read from and write into memory or I/Os.
Control and Status Signals

- **M1 Machine Cycle One:**
  - Status line indicates that an opcode is being fetched from memory.
  - Also used in an interrupt operation to generate an interrupt acknowledge signal.

![Diagram showing control and status signals](image)
Control and Status Signals

- MREQ Memory Request:
  - indicates that the address bus holds a valid address for a memory read or writes operation.
Control and Status Signals

- **IORQ I/O Request:**
  - Active low tri-state line
  - Indicates that the low-order address bus (A7 – A0) holds a valid address for an I/O read or writes operation.
Control and Status Signals

- **RD - Read:**
  - Indicates that the microprocessor is ready to read data from memory or an I/O device
  - Used in conjunction with **MREQ** for the Memory Read (**MEMRD**) operation
  - Used in conjunction with **IORQ** for the I/O Read (**IORD**) operation.
Control and Status Signals

- **WR—Write:**
  - Indicates that the microprocessor has already placed a data byte on the data bus and is ready to write into memory or an I/O device.
  - Should be used in conjunction with \( \overline{MREQ} \) for the Memory Write (\( \overline{MEMWR} \)) operation.
  - Should be used in conjunction with \( \overline{IORQ} \) for the I/O Write (\( \overline{IOWI} \)) operation.
External Requests

- Includes **five** different input signals to the microprocessor from external sources.

- Used to interrupt an ongoing process and to request the microprocessor to do something else.
External Requests

- **RESET**— Reset:
  
  - used to reset the microprocessor.
    - Clears the program counter (PC), the interrupt register (I), and the memory refresh register (R).
    - Everything is in reset state—e.g. address bus and the data bus are in high impedance state.
External Requests

- **INT—Interrupt Request:**
- initiated by an external I/O device to interrupt the microprocessor operation.
- When the microprocessor accepts the interrupt request, it acknowledges by activating **IORQ** the signal.
- The signal is maskable, meaning it can be disabled through a software instruction.
External Requests

- **NMI** – Nonmaskable Interrupt
  
  - It cannot be disabled. It is activated by a negative edge-triggered signal from an external source.
  - Used primarily for implementing emergency procedures.
  - No Ack signal is generated
External Requests

**BUSRQ – Bus Request:**

- Initiated by external I/O devices such as the DMA (Direct Memory Access) controller

- An I/O device can send a low signal to request the use of the address bus, the data bus, and the control signals.

- The external device can use the buses and when its operations are complete, it returns the control to the microprocessor.
External Requests

- **WAIT** – **Wait:**

- This signal is used when the response time of memory or I/O devices is slower than that of the Z80
Request Acknowledge and Special Signals

- **BUSAK**  **Bus Acknowledge**:

  - Initiated by the Z80 in response to the Bus Request signal.
  
  - Indicates to the requesting device that the address bus, the data bus, and the control signals have entered into the high impedance state and can be used by the requesting device.
Request Acknowledge and Special Signals

- **HALT** – **Halt**: Indicates that the MPU has executed the HALT instruction.
Request Acknowledge and Special Signals

- **RFSH – Refresh**: 
  - Indicating that the address bus $A_6-A_0$ (low-order seven bits) holds a refresh address of dynamic memory;
  - Should be used in conjunction with **MREQ** to refresh memory contents.
Power and Frequency Signals

- **Clock:**
  - Used to connect a single phase frequency source.

- The Z80 does not include a clock circuit on its chip.
+5V and GND:

- These pins are for a power supply and ground reference;
- The Z80 requires one +5V power source.
Z80 Programming Model

- Accumulator and a flag register,

- General-purpose register arrays, registers as memory pointers, and special-purpose registers.
General-Purpose Registers

- **Six** programmable general-purpose registers named B, C, D, E, H, and L

- 8-bit registers used for storing data during the program execution.

- can be combined as register pairs – BC, DE, and HL – to perform 16-bit operations or to hold memory addresses
Accumulator

- Part of the arithmetic logic unit (ALU) and is also identified as register A.

- The result of an operation performed in the ALU is stored in the accumulator.
Flag Register

- ALU includes six flip-flops that are set or reset according to data conditions after an ALU operation

- D0 - D7 are the ALU status flag
Alternate Register Set

- not directly available to the programmer
- Used for internal operations
16-Bit Registers As memory Pointers

- **four** 16-bit registers
- used to hold memory addresses
- **Index Registers (IX and IY)**
  - used to identify locations for data transfer.
- **Stack Pointer (SP)**
  - point to the memory location called the stack.
  - The stack is a defined area of memory location in R/W memory
16-Bit Registers As memory Pointers

- **Program Counter (PC)**
  - Used by MPU to sequence the execution of instructions

- **Special-Purpose Registers**
  - two special-purpose registers that are generally absent in other 8-bit microprocessors
  - Described later
Machine Cycles and Bus Timings

Next time