**Microprocessors**

**Z80 Structure**

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**Z80 Pin Assignment**

- M1 - Machine Cycle One (output, active Low).
- MREQ - Memory Request (output, active Low, 3-state).
- IORQ - Input/Output Request (output, active Low, 3-state).
- RD - Read (output, active Low, 3-state).
- WR - Write (output, active Low, 3-state).
- BUSREQ - Bus Request (input, active Low).
- BUSACK - Bus Acknowledge (output, active, Low).

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**Z80 Pin Description**

- **A15-A0**:
  - Address bus (output, active high, 3-state).
  - Used for accessing the memory and I/O ports.
  - During the refresh cycle the R is put on this bus.
- **D7-D0**:
  - Data Bus (input/output, active high, 3-state).
  - Used for data exchanged with memory, I/O.
- **RD**:
  - Read (output, active Low, 3-state) indicates that the CPU wants to read data from memory or I/O during the refresh cycle.
- **WR**:
  - Write (output, active Low, 3-state) indicates that the CPU data bus holds valid data to be stored at the addressed memory or I/O location.

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**Z80 Pin Description**

- **INT**:
  - Interrupt Request (input, active Low).
  - Checked at the end of the current instruction.
  - If flip-flop (IFF) is enabled.
- **NMI**:
  - Non-Maskable Interrupt.
  - Recognized at the end of the current instruction.
  - Independent of the status of IFF.
  - Forces the CPU to restart at location 0066H.

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**Z80 Pin Description**

- **MREQ**:
  - Memory Request (output, active Low, 3-state).
  - Indicates memory read/write operation. See M1.
- **IORQ**:
  - Input/Output Request (output, active Low, 3-state).
  - Indicates I/O read/write operation. See M1.
- **M1**:
  - Machine Cycle One (output, active Low).
  - Together with MREQ indicates opcode fetch cycle.
  - Together with IORQ indicates an Int Ack cycle.
- **RFSH**:
  - Refresh (output, active Low).
  - Together with MREQ indicates refresh cycle.
  - Lower 7-bits address is refresh address to DRAM.

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**Z80 Pin Description**

- **BUSREQ**:
  - Bus Request (input, active Low).
  - Higher priority than NMI.
  - Recognized at the end of the current machine cycle.
  - Forces the CPU address bus, data bus, and MREQ, IORQ, RD, and WR to high-imp.
- **BUSACK**:
  - Bus Acknowledge (output, active Low).
  - Indicates a requesting device that address, data, and control signals MREQ, IORQ, RD, and WR have entered their high-impedance states.
Z80 Pin Description

RESET
Reset (input, active Low).
RESET initializes the CPU as follows:
- Resets the IFF
- Clears the PC and registers I and R
- Sets the interrupt status to Mode 0.
During reset time, the address and data bus go to a high-impedance state. All control output signals go to the inactive state. Must be active for a minimum of three full clock cycles before the reset operation is complete.

BUS Buffering

Instruction Fetch

Memory Read or Write Cycle

Input or Output Cycles

Bus Request/Acknowledge Cycle